

## EAST SEARCH

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L#	Hits	Search String	Databases
L1	49	dual threshold voltage	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	432622	(integrated or digital) adj circuit\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	72	((integrated or digital) adj circuit\$1) and (dominant near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	256	((integrated or digital) adj circuit\$1) and (partial near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	0	3 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	43	dominant logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	19	2 and 6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	17	3 and (determin\$3 with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	4	3 and (determin\$3 with dominant with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	25	4 and (determin\$3 with partial with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	3	10 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	84	2 and (partial same (logic near2 state))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	30	4 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	0	12 and 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	4	2 and (partial near2 logic near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	15	2 and (partial with "logic state")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	3	2 and ("partial logic" with state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	0	2 and ("partial logic state")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	15960	((integrated or digital) adj circuit\$1) and (leakage near2 current\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	280	19 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	11	12 and partition\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	68	20 and (logic near2 state)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	1	22 and (partition\$1 same(logic near2 state))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	5	circuit design and "dual threshold voltage"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	1358	(dual or two or multiple) near2 "threshold voltage"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	40	25 and "circuit design" and (leakage near2 current\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	2	determin\$3 with "dominant state" with logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	93	25 and "circuit design"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	4	dominant logic state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	20	dominant state with logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	16	logic state with dominant	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	50	2 and (partition\$1 with "power supply")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	5	DC-connected component or "DC connected compo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

L34 0 2 and "cone of influence"  
L35 0 2 and "cone of transistors"

USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM\_TDB  
USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM\_TDB

09/580854 David Blaauw et al

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### Results of search set L33:((dual or two or multiple) near2 "threshold voltage") and "circuit design"

Document Kind	Codes	Title	Issue Date	Current OR	Abstract
US	20030170938 A1	Thin film semiconductor device and method for manufacturing same	20030911	438/166	
US	20030071315 A1	Reprogrammable non-volatile memory using a breakdown phenomena in an ultra-th	20030417	257/390	
US	20030071296 A1	Reprogrammable non-volatile memory using a breakdown phenomena in an ultra-th	20030417	257/298	
US	20030070147 A1	Dual threshold gate array or standard cell power saving library circuits	20030410	716/2	
US	20030006816 A1	Semiconductor integrated circuit device and microcomputer	20030109	327/158	
US	20020177279 A1	Method for making multiple threshold voltage fet using multiple work-function gate r	20021128	438/289	
US	20020175712 A1	CMOS skewed static logic and method of synthesis	20021128	326/98	
US	20020175643 A1	DUAL SIDED SELF-OSCILLATION CIRCUIT FOR DRIVING AN OSCILLATORY A	20021128	318/114	
US	20020154545 A1	Non-volatile memory device with plurality of threshold voltage distributions	20021024	365/185.22	
US	20020145174 A1	SOI FET and method for creating FET body connections with high-quality matching	20021010	257/510	
US	20020093064 A1	Semiconductor device and method of fabricating the same	20020718	257/408	
US	20020030521 A1	Semiconductor integrated circuit device and microcomputer	20020314	327/158	
US	20010022753 A1	Circuit and method for timing multi-level non-volatile memories	20010920	365/203	
US	6615229 B1	Dual threshold voltage complementary pass-transistor logic implementation of a low	20030902	708/629	
US	6608509 B1	Semiconductor integrated circuit device and microcomputer	20030819	327/149	
US	6597220 B2	Semiconductor integrated circuit device and microcomputer	20030722	327/158	
US	6593799 B2	Circuit including forward body bias from supply voltage and ground nodes	20030715	327/534	
US	6574146 B2	Circuit and method for timing multi-level non-volatile memories	20030603	365/185.2	
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US	6472916 B2	Semiconductor integrated circuit device and microcomputer	20021029	327/158	
US	6448590 B1	Multiple threshold voltage FET using multiple work-function gate materials	20020910	257/202	
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US	6388483 B1	Semiconductor integrated circuit device and microcomputer	20020514	327/158	
US	6373753 B1	Memory array having selected word lines driven to an internally-generated boosted	20020416	365/189.09	
US	6363029 B1	Semiconductor device incorporating internal power supply for compensating for dev	20020326	365/230.06	
US	6348713 B1	Method for fabricating semiconductor device	20020219	257/347	
US	6313511 B1	Semiconductor device	20011106	257/392	

US 6300819 B1	Circuit including forward body bias from supply voltage and ground nodes	20011009 327/534
US 6232827 B1	Transistors providing desired threshold voltage and reduced short channel effects v	20010515 327/537
US 6218895 B1	Multiple well transistor circuits having forward body bias	20010417 327/566
US 6208575 B1	Dynamic memory array bit line sense amplifier enabled to drive toward, but stoppe	20010327 365/208
US 6198314 B1	Sample and hold circuit and method therefor	20010306 327/94
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US 6161213 A	System for providing an integrated circuit with a unique identification	20001212 716/4
US 6128224 A	Method and apparatus for writing an erasable non-volatile memory	20001003 365/185.18
US 6125050 A	Configuration for driving parallel lines in a memory cell configuration	20000926 365/51
US 6100751 A	Forward body biased field effect transistor providing decoupling capacitance	20000808 327/534
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US 6073208 A	Apparatus and method for reducing programming cycles for multistate memory syst	20000606 711/103
US 6014327 A	Memory apparatus including programmable non-volatile multi-bit memory cell, and ;	20000111 365/185.03
US 6014044 A	Voltage comparator with floating gate MOS transistor	20000111 327/81
US 5912571 A	Using the internal supply voltage ramp rate to prevent premature enabling of a devi	19990615 327/143
US 5907855 A	Apparatus and method for reducing programming cycles for multistate memory syst	19990525 711/103
US 5831451 A	Dynamic logic circuits using transistors having differing threshold voltages	19981103 326/93
US 5821778 A	Using cascode transistors having low threshold voltages	19981013 326/95
US 5815446 A	Potential generation circuit	19980929 365/189.09
US 5815005 A	Power reduction circuits and systems for dynamic logic gates	19980929 326/95
US 5793698 A	Semiconductor read-only VLSI memory	19980811 365/230.08
US 5774367 A	Method of selecting device threshold voltages for high speed and low power	19980630 716/2
US 5757055 A	Triple drain magneto field effect transistor with high conductivity central drain	19980526 257/421
US 5751635 A	Read circuits for analog memory cells	19980512 365/185.19
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US 5638320 A	High resolution analog storage EPROM and flash EPROM	19970610 365/185.03
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US 5374859 A	Low power dual power supply high resolution comparator	19941220 327/65
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US 4492224 A	Dynamic merged load logic (MLL) and merged load memory (MLM)	19840515 377/79
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US 4434479 A	Nonvolatile memory sensing system	19840228 365/210
US 4417325 A	Highly scaleable dynamic ram cell with self-signal amplification	19831122 365/185.08
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US 3989034 A	Apparatus and method for signaling fetal distress and uterine contraction monitor	19761102 600/511
US RE28905 E	Field effect transistor memory cell	19760713 365/190
US 3903431 A	Clocked dynamic inverter	19750902 326/88
US 3845324 A	DUAL VOLTAGE FET INVERTER CIRCUIT WITH TWO LEVEL BIASING	19741029 326/119
US 3794999 A	NOISE-FIGURE MEASURING CIRCUIT	19740226 342/168
US 3663835 A	FIELD EFFECT TRANSISTOR CIRCUIT	19720516 327/581
US 20020018362 A	Programmable circuit for DRAM, has latch circuit which applies threshold voltage to	20020214

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Then click **Search Again**.**Results:**Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 Technology of a depth-2 full-adder circuit using the InP RTD/HFET MOBILE***Prost, W.; Auer, U.; Degenhardt, J.; Brennemann, A.; Pacha, C.; Goser, K.F.; Tegude, F.-J.;*

Indium Phosphide and Related Materials, 2001. IPRM. IEEE International Conference On , 14-18 May 2001

Page(s): 228 -231

[\[Abstract\]](#) [\[PDF Full-Text \(412 KB\)\]](#) **IEEE CNF****2 Dual threshold voltage circuits in the presence of resistive interconnects***Larsson-Edefors, P.; Eckerbert, D.; Eriksson, H.; Svensson, L.J.;*

VLSI, 2003. Proceedings. IEEE Computer Society Annual Symposium on , 20-21 Feb. 2003

Page(s): 225 -230

[\[Abstract\]](#) [\[PDF Full-Text \(303 KB\)\]](#) **IEEE CNF****3 Dual threshold delay model for nonlinear device characterization***Tomita, Y.; Iwanishi, N.; Yamaguchi, R.; Edamatsu, H.;*

Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , 1-4 May 1995

Page(s): 371 -374

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) **IEEE CNF**

#### **4 Low power synthesis of dual threshold voltage CMOS VLSI circuits**

*Sundararajan, V.; Parhi, K.K.;*

Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on , 16-17 Aug. 1999

Page(s): 139 -144

[\[Abstract\]](#) [\[PDF Full-Text \(392 KB\)\]](#) [IEEE CNF](#)

---

#### **5 Design methodology and optimization strategy for dual- $V_{TH}$ scheme using commercially available tools**

*Hirabayashi, M.; Nose, K.; Sakurai, T.;*

Low Power Electronics and Design, International Symposium on, 2001. , 6-7 Aug. 2001

Page(s): 283 -286

[\[Abstract\]](#) [\[PDF Full-Text \(292 KB\)\]](#) [IEEE CNF](#)

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#### **6 Low-swing clock domino logic incorporating dual supply and dual threshold voltages**

*Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;*

Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(693 KB\)\]](#) [IEEE CNF](#)

---

#### **7 Long-term power minimization of dual- $V_{sub T}$ CMOS circuits**

*Suhwan Kim; Youngsoo Shin; Kosonocky, S.; Wei Hwang;*

ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 2002

Page(s): 323 -327

[\[Abstract\]](#) [\[PDF Full-Text \(378 KB\)\]](#) [IEEE CNF](#)

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#### **8 Dual threshold voltage domino logic synthesis for high performance with noise and power constraint**

*Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;*

Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings , 4-8 March 2002

Page(s): 260 -265

[\[Abstract\]](#) [\[PDF Full-Text \(270 KB\)\]](#) [IEEE CNF](#)

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**9 Technology mapping for low leakage power and high speed with hot-carrier effect consideration**

*Chang-woo Kang; Pedram, M.;*

Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific , 21-24 Jan. 2003

Page(s): 203 -208

[\[Abstract\]](#) [\[PDF Full-Text \(699 KB\)\]](#) **IEEE CNF**

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**10 Dual-threshold voltage techniques for low-power digital circuits**

*Kao, J.T.; Chandrakasan, A.P.;*

Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 7 , July 2000

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[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) **IEEE JNL**

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**11 Dual-threshold voltage assignment with transistor sizing for low power CMOS circuits**

*Pant, P.; Roy, R.K.; Chatterjee, A.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 Issue: 2 , April 2001

Page(s): 390 -394

[\[Abstract\]](#) [\[PDF Full-Text \(144 KB\)\]](#) **IEEE JNL**

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**12 Leakage power analysis and reduction during behavioral synthesis**

*Khouri, K.S.; Jha, N.K.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 Issue: 6 , Dec. 2002

Page(s): 876 -885

[\[Abstract\]](#) [\[PDF Full-Text \(531 KB\)\]](#) **IEEE JNL**

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**13 Noise constrained transistor sizing and power optimization for dual V/sub t/ domino logic**

*Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 Issue: 5 , Oct. 2002

Page(s): 532 -541

[\[Abstract\]](#) [\[PDF Full-Text \(769 KB\)\]](#) **IEEE JNL**

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**14 Energy-efficient skewed static logic with dual Vt: design and synthesis**

*Chulwoo Kim; Ki-Wook Kim; Sung-Mo Kang;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on ,  
Volume: 11 Issue: 1 , Feb. 2003

Page(s): 64 -70

[\[Abstract\]](#) [\[PDF Full-Text \(508 KB\)\]](#) **IEEE JNL**

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**15 Timing constraints for domino logic gates with timing-dependent keepers**

*Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE  
Transactions on , Volume: 22 Issue: 1 , Jan. 2003

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[\[Abstract\]](#) [\[PDF Full-Text \(473 KB\)\]](#) **IEEE JNL**

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- 1 [Energy and Delay Considerations: Low swing dual threshold voltage domino logic](#) 82%  
 Volkan Kursun , Eby G. Friedman  
**Proceedings of the 12th ACM Great Lakes Symposium on VLSI April 2002**  
 A low swing domino logic technique is proposed to decrease power consumption without sacrificing noise immunity. With the proposed low swing domino logic circuit technique, active power consumption is reduced by up to 9.4% while improving the noise immunity by 2.6% as compared to standard domino logic circuits. It is also shown that by applying a low swing contention reduction technique, the power savings can be further increased by 6.7% while the delay can be improved by 8.6%. A simple and effi ...
- 2 [Transistor sizing for reliable domino logic design in dual threshold voltage technologies](#) 82%  
 Seong-Ook Jung , Ki-Wook Kim , Sung-Mo Steve Kang  
**Proceedings of the 11th Great Lakes Symposium on VLSI March 2001**
- 3 [Energy aware design: Managing static leakage energy in microprocessor functional units](#) 80%  
 Steven Dropsho , Volkan Kursun , David H. Albonesi , Sandhya Dwarkadas , Eby G. Friedman  
**Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture November 2002**  
 Static energy due to subthreshold leakage current is projected to become a major component of the total energy in high performance microprocessors. Many studies so far have examined and proposed techniques to reduce leakage in on-chip storage structures. In this study, static energy is reduced in the integer functional units by leveraging the unique qualities of dual threshold voltage domino logic. Domino logic has desirable properties that greatly reduce leakage current while providing fast prop ...
- 4 [Low-power physical design: Low-swing clock domino logic incorporating dual supply and dual threshold voltages](#) 80%  
 Seong-Ook Jung , Ki-Wook Kim , Sung-Mo Kang  
**Proceedings of the 39th conference on Design automation June 2002**

High-speed domino logic is now prevailing in performance critical block of a chip. Low Voltage Swing Clock (LVSC) domino logic family is developed for substantial dynamic power saving. To boost up the transition speed in proposed circuitry, a well-established dual threshold voltage technique is exploited. Dual supply voltage technique in the LVSC domino logic is geared to reduce power consumption in clock tree and logic gates effectively. Delay Constrained Power Optimization (DCPO) algorithm all ...

**5 Coupling delay optimization by temporal decorrelation using dual threshold voltage technique** 80%

**4** Ki-Wook Kim , Seong-Ook Jung , Prashant Saxena , C. L. Liu , Sung-Mo Kang

**Proceedings of the 38th conference on Design automation** June 2001

Coupling effect due to line-to-line capacitance is of serious concern in timing analysis of circuits in ultra deep submicron CMOS technology. Often coupling delay is strongly dependent on temporal correlation of signal switching in relevant wires. Temporal decorrelation by shifting timing window can alleviate performance degradation induced by tight coupling. This paper presents an algorithm for minimizing circuit delay through timing window modulation in dual  $V_{th}$  technology. Experimental ...

**6 Keynote speech 1: Elements of low power design for integrated systems** 77%

**4** Sung-Mo Kang

**Proceedings of the 2003 international symposium on Low power electronics and design**  
August 2003

The increasing prominence of portable systems and the need to limit power consumption and hence, heat dissipation in very high density VLSI chips have led to rapid and innovative developments in low power design recently. Leakage control is becoming critically important for deep sub-100nm technologies due to the scaling down of threshold voltage and gate oxide thickness of transistors. In this paper, we discuss major sources of power dissipation in VLSI systems, and various low power design tech ...

**7 Advances in low power synthesis: Minimization of dynamic and static power through joint** 77%

**4** assignment of threshold voltages and sizing optimization

David Nguyen , Abhijit Davare , Michael Orshansky , David Chinnery , Brandon Thompson , Kurt Keutzer

**Proceedings of the 2003 international symposium on Low power electronics and design**  
August 2003

We describe an optimization strategy for minimizing total power consumption using dual threshold voltage ( $V_{th}$ ) technology. Significant power savings are possible by simultaneous assignment of  $V_{th}$  with gate sizing. We propose an efficient algorithm based on linear programming that jointly performs  $V_{th}$  assignment and gate sizing to minimize total power under delay constraints. First, linear programming assigns the optimal amounts of slack to gates based on power-delay sensitivity. Then, an optimal ...

**8 Design strategies for controlling standby leakage: Design methodology for fine-grained leakage** 77%

**4** control in MTCMOS

Benton H. Calhoun , Frank A. Honore , Anantha Chandrakasan


**Proceedings of the 2003 international symposium on Low power electronics and design**  
August 2003

Multi-threshold CMOS is a popular technique for reducing standby leakage power with low delay overhead. MTCMOS designs typically use large sleep devices to reduce standby leakage at the

block level. We provide a formal examination of sneak leakage paths and a design methodology that enables gate-level insertion of sleep devices for sequential and combinational circuits. A fabricated 0.13  $\mu$ m, dual V<sub>T</sub> testchip employs this methodology to implement a low-power FPGA core with gate-level sleep ...

9 VLSI circuits: Reduced dynamic swing domino logic

77%


 Roy Mader , Ivan Kourtev

**Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003**

A new reduced-swing domino logic technique is presented which provides significantly lower power dissipation as compared to traditional domino circuit structures. Additionally, the noise margins of the new circuit offer an improvement over standard domino design. The key idea of the new design style is to limit both the upper and lower bounds of the voltage swing at the internal dynamic node. The voltage swing at the inputs and the outputs of the domino circuit remains full-swing. A number of ci ...

10 Standby power optimization via transistor sizing and dual threshold voltage assignment

77%


 Mahesh Ketkar , Sachin S. Sapatnekar

**Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design November 2002**

This paper presents a novel enumerative approach, with provable and efficient pruning techniques, for dual threshold voltage (V<sub>t</sub>) assignment at the transistor level. Since the use of low V<sub>t</sub> may entail a substantial increase in leakage power, we formulate the problem as one of combined optimization for leakage-delay tradeoffs under V<sub>t</sub> optimization and sizing. Based on an analysis of the effects of these two transforms on the delay and leakage, ...

11 Multi-voltage, multi-threshold design: Total power optimization by simultaneous dual-V<sub>t</sub> allocation and device sizing in high performance microprocessors

77%


 Tanay Karnik , Yibin Ye , James Tschanz , Liqiong Wei , Steven Burns , Venkatesh Govindarajulu , Vivek De , Shekhar Borkar

**Proceedings of the 39th conference on Design automation June 2002**

We describe various design automation solutions for design migration to a dual-V<sub>t</sub> process technology. We include the results of a Lagrangian Relaxation based tool, iSTATS, and a heuristic iterative optimization flow. Joint dual-V<sub>t</sub> allocation and sizing reduces total power by 10+% compared with V<sub>t</sub> allocation alone, and by 25+% compared with pure sizing methods. The heuristic flow requires 5x larger computation runtime than iSTATS due to its iterative nature.

12 Future performance challenges in nanometer design

77%


 Dennis Sylvester , Himanshu Kaul

**Proceedings of the 38th conference on Design automation June 2001**

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes < 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-V<sub>dd</sub> + multi-V<sub>th</sub> + re-sizing approach is advocated to leverage the inherent pr ...

13 A static power model for architects

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 J. Adam Butts , Gurindar S. Sohi

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